REMARKS

Claims 1 through 55 are currently pending in the application.

Claims 6 through 55 are withdrawn from consideration as being directed to a non-elected invention. Claims 1 through 5 are rejected.

This amendment is in response to the Office Action of February 4, 2004.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on D'Souza (U.S. Patent 5,323,107) in view of Bierig (U.S. Patent 4,089,734) and further in view of Rostoker et al. (U.S. Patent 5,838,163)

Claims 1 through 3 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over D'Souza (U.S. Patent 5,323,107) in view of Bierig (U.S. Patent 4,089,734) and further in view of Rostoker et al. (U.S. Patent 5,838,163). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Turning to the cited prior art, the D'Souza reference teaches a probe card having integral circuitry directly attached to the probe card with some of the circuitry including fuse elements used to program the probe card for use with different types of semiconductor devices.

The Bierig reference teaches the use of an integrated circuit fusing technique for use on an integrated circuit substrate. In a read only memory employing integrated circuit fuses it is necessary to blow a fuse at the corresponding location in the diode storage matrix on the read only memory semiconductor chip. It is important in that application that the fuses blow at a pre-specified current; otherwise the entire unit will be prone to failure. If the fuse were to blow at

too low a current, the fuse could blow during normal device operation resulting in a change of stored data. If the furs were to require too large current to blow, it would not be possible to program the correct data into the memory as t limited amount of current is typically available from driving devices used to blow the fuse.

The Rostoker et al. reference teaches the use of fuses in the circuitry of an unsigulated wafer of semiconductor devices to protect against various faults which may occur in the conductive lines of the wafer.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant has amended the claimed invention to clearly distinguish over the cited prior art.

Applicant asserts that any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention because any combination of the cited prior art fails, at the very least, teach or suggest all of the claim limitations and fails to have any suggestion to make the claimed combination and the reasonable expectation of success both found in the prior art, and not based on Applicant's disclosure.

Applicant asserts that any combination of the cited prior art fails to teach or suggest the claim limitations of the presently claimed invention of presently amended independent claim 1 calling for "providing a plurality of fuse elements in respective electrical communication with at least some of the plurality of conductive traces, at least some of the plurality of fuse elements disposed immediately adjacent the at least one of the first surface and the second surface, at least some of said plurality of fuse elements comprising at least two types of fuses of an active fuse element, a passive fuse element, a self-resetting fuse element, a repairable fuse element, and a replaceable fuse element, each fuse element of the plurality of fuse elements for limiting the current level thereof to one of an absolute maximum current level for the probe card without substantial damage thereto and an absolute current level for use in the testing of a semiconductor device without substantial damage thereto".

In contrast to the claim limitations of the presently claimed invention of presently amended independent claim 1, the D'Souza reference uses the fuses to program the probe card

for use with different types of semiconductor devices. The Bierig reference uses the fuses for programming a read only memory. The Rostoker et al. reference used the fuses for testing semiconductor devices while still in wafer form with the fuses formed on the wafer. Applicant asserts that any combination of the cited prior art results in the D'Souza probe card having fuses that are capable of being blown at very precise current levels used to program the probe card for use in testing different types of semiconductor devices in wafer form with the wafer also including fuses in the circuitry thereof. Such is not the presently claimed invention requiring the ". . . a plurality of fuse elements in respective electrical communication with at least some of the plurality of conductive traces, at least some of the plurality of fuse elements disposed immediately adjacent the at least one of the first surface and the second surface, at least some of said plurality of fuse elements comprising at least two types of fuses of an active fuse element, a passive fuse element, a self-resetting fuse element, a repairable fuse element, and a replaceable fuse element, each fuse element of the plurality of fuse elements for limiting the current level thereof to one of an absolute maximum current level for the probe card without substantial damage thereto and an absolute current level for use in the testing of a semiconductor device without substantial damage thereto". Accordingly, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of presently amended independent claim 1. Therefore, presently amended independent claim 1 and dependent claims 2 through 5 therefrom are allowable.

Applicant asserts further that any rejection of the presently claimed invention based upon any combination of the cited prior art also fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention because any such combination of the cited prior art fails to have any suggestion to make the claimed combination and fails to have any showing of a reasonable expectation of success. Applicant asserts that the suggestion for the combination of the cited prior art and any expectation for success of the combination are both found solely in Applicant's disclosure, not the cited prior art. There is no suggestion whatsoever in any of the cited prior art to modify the D'Souza reference for any reason. Solely any reason and any expectation of success for any modification of the D'Souza reference are solely contained within Applicant's disclosure, not the cited prior art. As such, any combination

of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of presently amended independent claim 1. Therefore, presently amended independent claim 1 and dependent claims 2 through 5 therefrom are allowable.

Obviousness Rejection Based on D'Souza (U.S. Patent 5,323,107)/Bierig (U.S. Patent 4,089,734)/Rostoker et al. (U.S. Patent 5,838,163) as applied to claims 1 and 3 above, and further in view of Maruyama et al. (U.S. Patent 5,832,595)

Claims 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over D'Souza (U.S. Patent 5,323,107)/Bierig (U.S. Patent 4,089,734)/Rostoker et al. (U.S. Patent 5,838,163) as applied to claims 1 and 3 above, and further in view of Maruyama et al. (U.S. Patent 5,832,595). Applicant respectfully traverses this rejection, as hereinafter set forth.

Applicant AGAIN asserts that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

Again turning to the cited prior art, the D'Souza reference teaches a probe card having integral circuitry directly attached to the probe card with some of the circuitry including fuse elements used to program the probe card for use with different types of semiconductor devices.

The Bierig reference teaches the use of an integrated circuit fusing technique for use on an integrated circuit substrate. In a read only memory employing integrated circuit fuses it is necessary to blow a fuse at the corresponding location in the diode storage matrix on the read only memory semiconductor chip. It is important in that application that the fuses blow at a pre-specified current; otherwise the entire unit will be prone to failure. If the fuse were to blow at too low a current, the fuse could blow during normal device operation resulting in a change of

stored data. If the furs were to require too large current to blow, it would not be possible to program the correct data into the memory as t limited amount of current is typically available from driving devices used to blow the fuse.

The Rostoker et al. reference teaches the use of fuses in the circuitry of an unsigulated wafer of semiconductor devices to protect against various faults which may occur in the conductive lines of the wafer.

The Maruyama et al. reference teaches the use of copper for circuits of a circuit board.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant has amended the claimed invention to clearly distinguish over the cited prior art.

Applicant asserts that any combination of the cited prior art fails to teach or suggest the claim limitations of the presently claimed invention of presently amended independent claim 1 calling for "providing a plurality of fuse elements in respective electrical communication with at least some of the plurality of conductive traces, at least some of the plurality of fuse elements disposed immediately adjacent the at least one of the first surface and the second surface, at least some of said plurality of fuse elements comprising at least two types of fuses of an active fuse element, a passive fuse element, a self-resetting fuse element, a repairable fuse element, and a replaceable fuse element, each fuse element of the plurality of fuse elements for limiting the current level thereof to one of an absolute maximum current level for the probe card without substantial damage thereto and an absolute current level for use in the testing of a semiconductor device without substantial damage thereto".

In contrast to the claim limitations of the presently claimed invention of presently amended independent claim 1, the D'Souza reference uses the fuses to program the probe card for use with different types of semiconductor devices. The Bierig reference uses the fuses for programming a read only memory. The Rostoker et al. reference used the fuses for testing semiconductor devices while still in wafer form with the fuses formed on the wafer. Applicant asserts that any combination of the cited prior art results in the D'Souza probe card having fuses that are capable of being blow at very precise current levels used to program the probe card for use in testing different types of semiconductor devices in wafer form with the wafer also

including fuses in the circuitry thereof. The Maruyama et al. reference teaches the use of copper for circuits of a circuit board. Such is not the presently claimed invention requiring the ". . . a plurality of fuse elements in respective electrical communication with at least some of the plurality of conductive traces, at least some of the plurality of fuse elements disposed immediately adjacent the at least one of the first surface and the second surface, at least some of said plurality of fuse elements comprising at least two types of fuses of an active fuse element, a passive fuse element, a self-resetting fuse element, a repairable fuse element, and a replaceable fuse element, each fuse element of the plurality of fuse elements for limiting the current level thereof to one of an absolute maximum current level for the probe card without substantial damage thereto and an absolute current level for use in the testing of a semiconductor device without substantial damage thereto" and is certainly not the claimed invention of dependent claim 4 having claim limitations calling for "the at least one fuse element of the plurality of fuse elements is formed of a material selected from the group consisting of titanium tungsten, aluminum, platinum silicide, copper, nichrome, doped polysilicon, metal silicide, and alloys of any thereof". Accordingly, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention of presently amended independent claim 1. Therefore, presently amended independent claim 1 and dependent claims 2 through 5 therefrom are allowable.

Applicant again asserts further that any rejection of the presently claimed invention based upon any combination of the cited prior art also fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the presently claimed invention because any such combination of the cited prior art fails to have any suggestion to make the claimed combination and the reasonable expectation of success. Applicant asserts that the suggestion for the combination of the cited prior art and any expectation for success of the combination are both found solely in Applicant's disclosure, not the cited prior art. There is no suggestion whatsoever in any of the cited prior art to modify the D'Souza reference for any reason. Solely any reason and any expectation of success for any modification of the D'Souza reference are solely contained within Applicant's disclosure, not the cited prior art. As such, any combination of the cited prior art does not and cannot establish a *prima facie* case of obviousness under 35 U.S.C. §

103 regarding the presently claimed invention of presently amended independent claim 1. Therefore, presently amended independent claim 1 and dependent claims 2 through 5 therefrom are allowable.

Applicant submits that claims 1 through 21 are clearly allowable over the cited prior art.

Applicant requests the allowance of claims 1 through 21 and the case passed for issue.

Respectfully submitted,

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